**HW1**

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**(a) What are the various IC foundries that offer their services through MOSIS?**

They are GlobalFoundries, TSMC, ams AG, ON Semi, AIM Photonics and imec-ePIXfab.

**(b) What are the feature sizes of the available fabrication processes?**

[GlobalFoundries](https://www.mosis.com/vendors/view/global-foundries) featured processes:

CMOS:[14 nm](https://www.mosis.com/vendors/view/global-foundries/014), [28 nm](https://www.mosis.com/vendors/view/global-foundries/028), [40 nm](https://www.mosis.com/vendors/view/global-foundries/040), [65 nm](https://www.mosis.com/vendors/view/global-foundries/n65), [0.13 µm](https://www.mosis.com/vendors/view/global-foundries/013) and [0.18 µm](https://www.mosis.com/vendors/view/global-foundries/018)

[TSMC](https://www.mosis.com/vendors/view/tsmc) featured processes:

[28 nm](https://www.mosis.com/vendors/view/tsmc/28nm), [40](https://www.mosis.com/vendors/view/tsmc/40nm) / [45 nm](https://www.mosis.com/vendors/view/tsmc/45nm), [65 nm](https://www.mosis.com/vendors/view/tsmc/65nm), [90 nm](https://www.mosis.com/vendors/view/tsmc/90nm), [130 nm](https://www.mosis.com/vendors/view/tsmc/013-cr), [180 nm](https://www.mosis.com/vendors/view/tsmc/018) and [350 nm](https://www.mosis.com/vendors/view/tsmc/035).

[ams AG](https://www.mosis.com/vendors/view/ams) featured processes:

0.18 µm in both [CMOS](https://www.mosis.com/vendors/view/ams/c18) and [HV CMOS](https://www.mosis.com/vendors/view/ams/h18)

[0.35 µm](https://www.mosis.com/vendors/view/ams/c35b_compare)

[ON Semi](https://www.mosis.com/vendors/view/on-semiconductor) featured CMOS processes

[I3T80 (0.35 µm)](https://www.mosis.com/vendors/view/on-semiconductor/i3t80), [C5 (0.5 µm)](https://www.mosis.com/vendors/view/on-semiconductor/c5), and [I2T100 (0.7 µm)](https://www.mosis.com/vendors/view/on-semiconductor/i2t100) CMOS

**For question (c), use the following processes only:**

**ON (0.5um CMOS)**

**AMS (0.18um CMOS)**

**GlobalFoundries (0.18um HV CMOS)**

**TSMC (90nm Mixed Signal G CMOS)**

**(c) Assuming that each transistor occupies an area of 12L x 16L, where L is (feature size)/2. How many transistors can be placed in each 5mm x 5mm chip offered by MOSIS.**

ON:

0.5um=0.0005mm

Row: 5/(12\*0.0005/2)=1666

Column: 5/(16\*0.0005/2)=1250

No. of transistors can be put on the 5mm\*5mm chip= 1666\*1250=2082500

AMS & GlobalFoundries:

0.18um=0.00018mm

Row: 5/(12\*0.00018/2)=4629

Column: 5/(16\*0.00018/2)=3472

No. of transistors can be put on the 5mm\*5mm chip= 3472\*4629=16071888

TSMC:

90nm=0.00009mm

Row: 5/(12\*0.00009/2)=9259

Column: 5/(16\*0.00009/2)=6944

No. of transistors can be put on the 5mm\*5mm chip= 9259\*6944=64294496

**(d) What is the value of COX, mobility and threshold voltage for the NMOS and PMOS transistors in the ON Semiconductor 0.5um run (wafer electrical tests sheet given below). Determine the capacitance between two 1mm long conductors, implemented with minimum width Poly1 and Metal3, drawn directly on top of each other.**

**Cox:**

NMOS: 57.2\*⅖=22.92 ua/v^3

PMOS: -18.9\*⅖=-7.56 ua/v^3

**Mobility**:

NMOS: 464.63 cm^2/vs

PMOS: 153.26 cm^2/vs

**Threshold Voltage: unit: v**

|  |  |  |
| --- | --- | --- |
|  | NMOS | PMOS |
| min | 0.78 | -0.88 |
| short | 0.67 | -0.86 |
| large | 0.68 | -0.73 |

Capacitance:

1mm=1000um

C= 9\*1000\*1000=9\*10^6 aF